



# PEMB24

50 V, 20 mA PNP/PNP resistor-equipped transistor;  
R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$

10 July 2023

Product data sheet

## 1. General description

PNP/PNP Resistor-Equipped Transistor (RET) in a SOT666 ultra small and flat lead Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PEMH24

NPN/PNP complement: PEMD24

## 2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place cost

## 3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replacement of general-purpose transistors in digital applications

## 4. Quick reference data

Table 1. Quick reference data

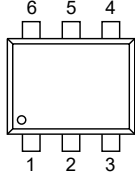
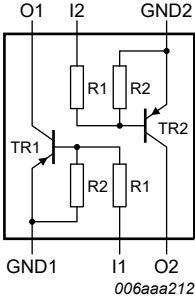
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V	
I <sub>O</sub>	output current		-	-	-20	mA	
R1	bias resistor 1 (input)		[1]	70	100	130	k $\Omega$
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See Section "Test information" for resistor calculation and test conditions.

50 V, 20 mA PNP/PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p style="text-align: center;"><b>SOT666</b></p>	 <p style="text-align: center;">006aaa212</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PEMB24</a>	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	<a href="#">SOT666</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PEMB24	6M

## 8. Limiting values

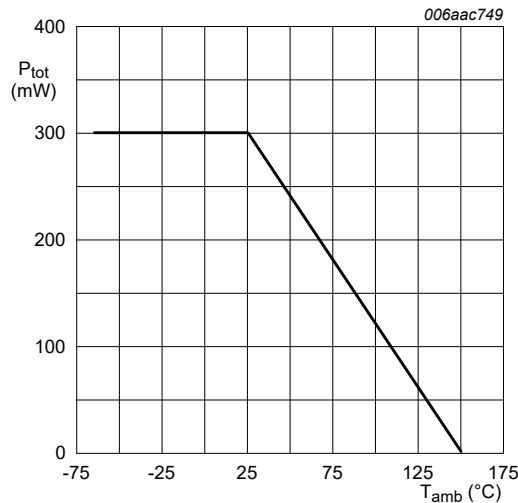
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
$V_{CBO}$	collector-base voltage	open emitter		-	-50	V
$V_{CEO}$	collector-emitter voltage	open base		-	-50	V
$V_{EBO}$	emitter-base voltage	open collector		-	-10	V
$V_I$	input voltage			-40	10	V
$I_O$	output current			-	-20	mA
$I_{CM}$	peak collector current			-	-100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1] [2]	-	200	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1] [2]	-	300	mW
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-65	150	°C
$T_{stg}$	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

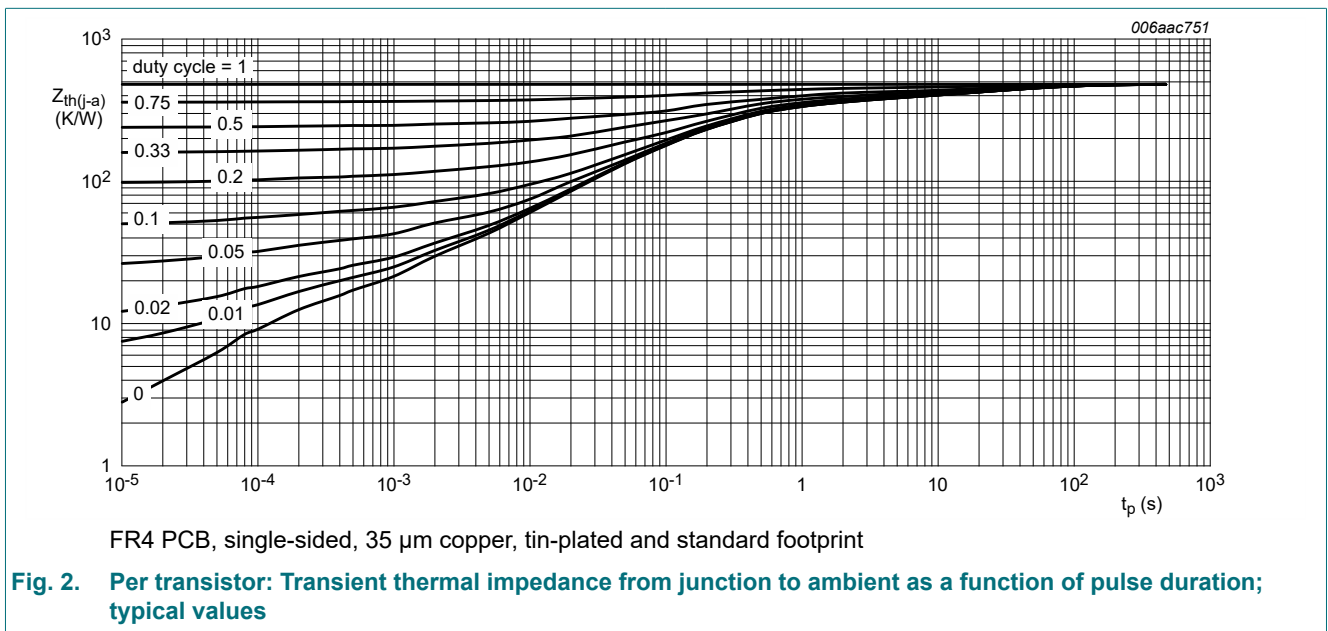
**Fig. 1. Per device: Power derating curve**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	416	K/W

- [1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Reflow soldering is the only recommended soldering method.

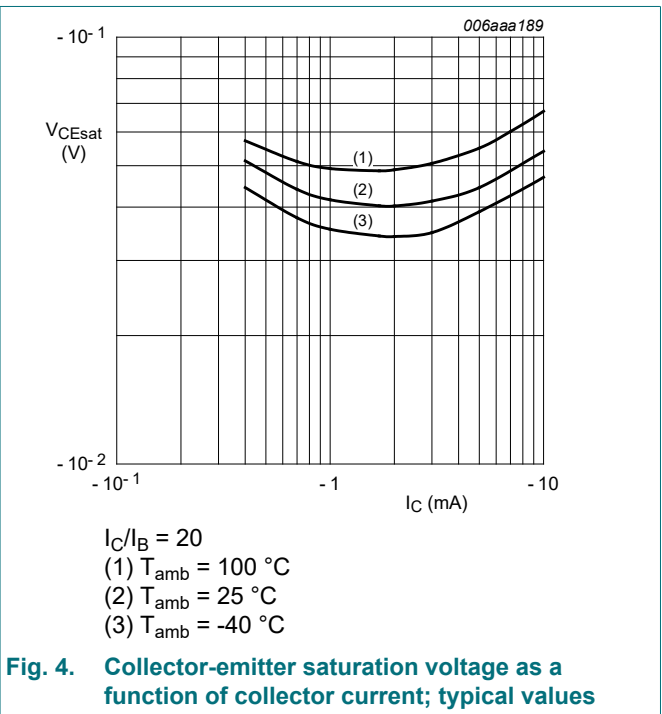
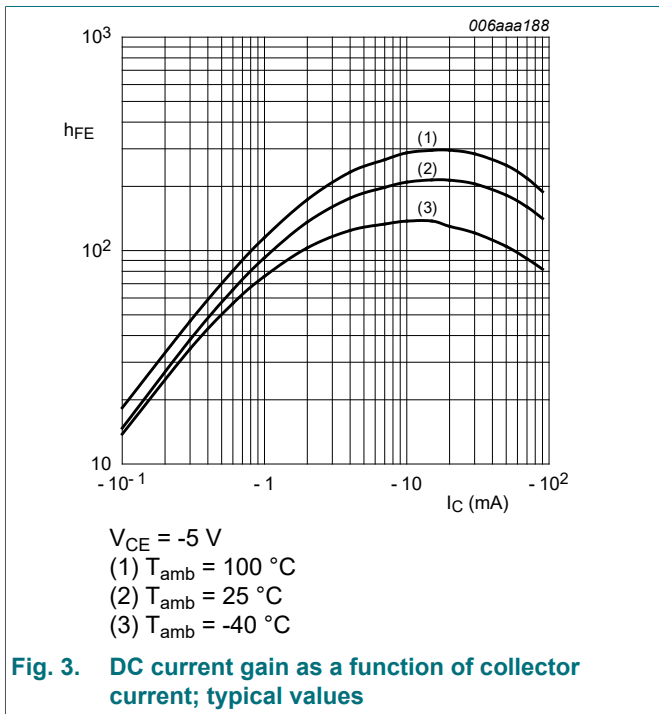


## 10. Characteristics

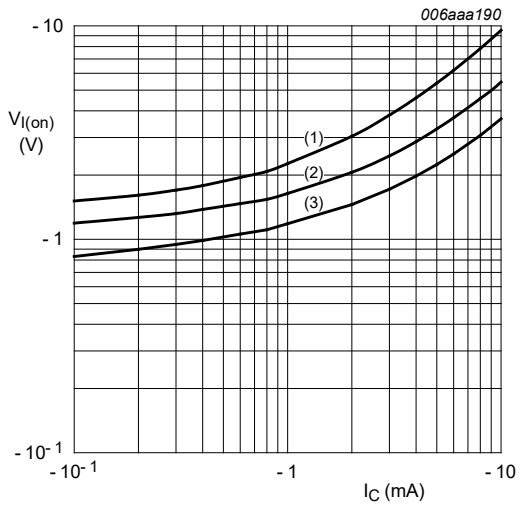
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A$ ; $I_E = 0 A$ ; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}$ ; $I_B = 0 A$ ; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -50 \text{ V}$ ; $I_E = 0 A$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$ ; $I_B = 0 A$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-	-1	$\mu A$	
		$V_{CE} = -30 \text{ V}$ ; $I_B = 0 A$ ; $T_j = 150 \text{ }^\circ C$	-	-	-50	$\mu A$	
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5 \text{ V}$ ; $I_C = 0 A$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-	-50	$\mu A$	
$h_{FE}$	DC current gain	$V_{CE} = -5 \text{ V}$ ; $I_C = -5 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ C$	80	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -5 \text{ mA}$ ; $I_B = -0.25 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-	-150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}$ ; $I_C = -100 \mu A$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-1.2	-0.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V}$ ; $I_C = -1 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ C$	-3	-1.6	-	V	
R1	bias resistor 1 (input)		[1]	70	100	130	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
$C_c$	collector capacitance	$V_{CB} = -10 \text{ V}$ ; $I_E = 0 A$ ; $i_e = 0 A$ ; $f = 1 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^\circ C$	-	-	2.5	pF	

[1] See Section "Test information" for resistor calculation and test conditions.

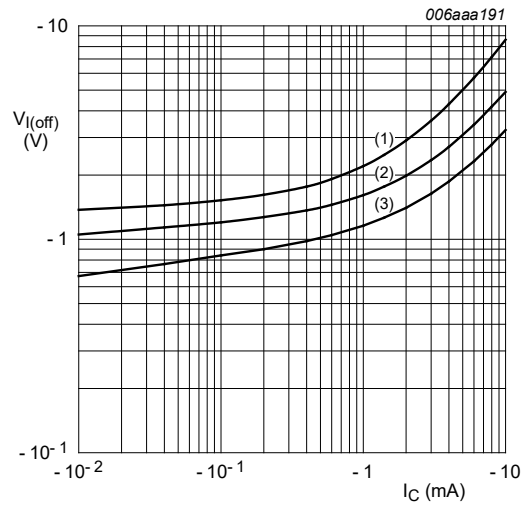


50 V, 20 mA PNP/PNP resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ



$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ °C}$   
 (2)  $T_{amb} = 25 \text{ °C}$   
 (3)  $T_{amb} = 100 \text{ °C}$

**Fig. 5. On-state input voltage as a function of collector current; typical values**



$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ °C}$   
 (2)  $T_{amb} = 25 \text{ °C}$   
 (3)  $T_{amb} = 100 \text{ °C}$

**Fig. 6. Off-state input voltage as a function of collector current; typical values**

## 11. Test information

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_3)}{R_1 \cdot I_3} - 1$$

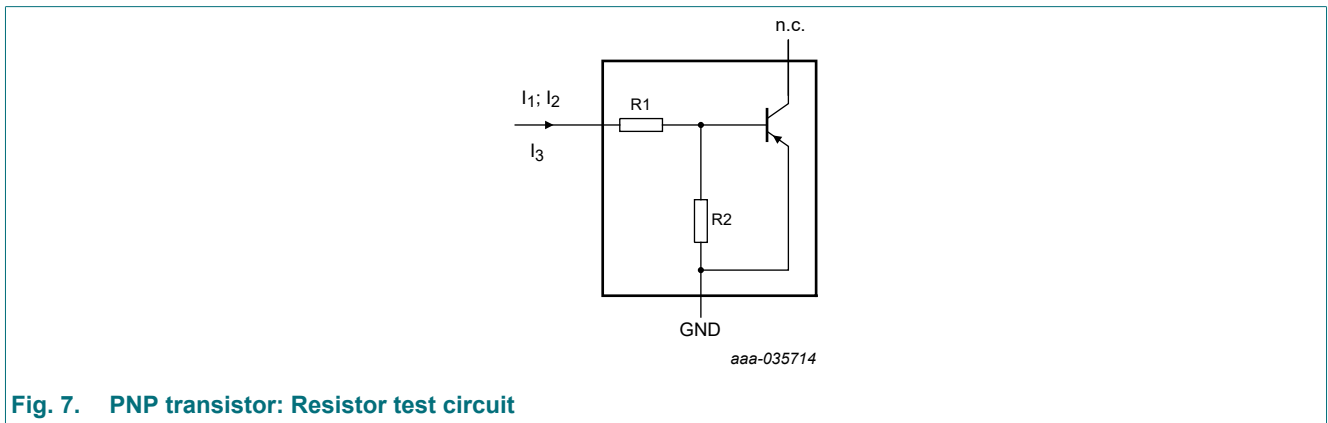


Fig. 7. PNP transistor: Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>
PEMB24	100	100	-20 μA	-60 μA	40 μA

## 12. Package outline

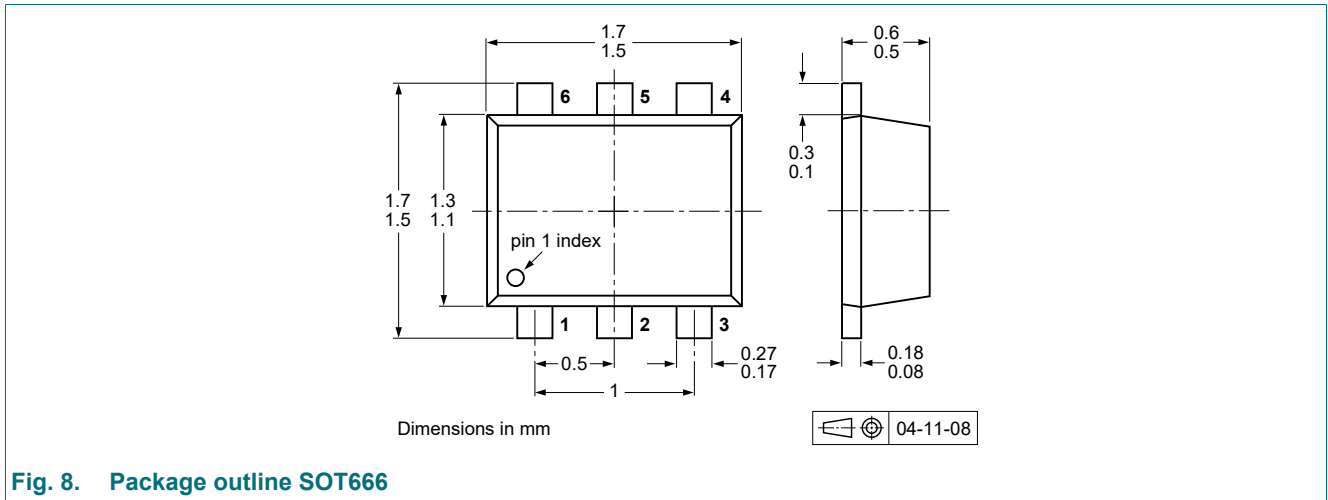


Fig. 8. Package outline SOT666

## 13. Soldering

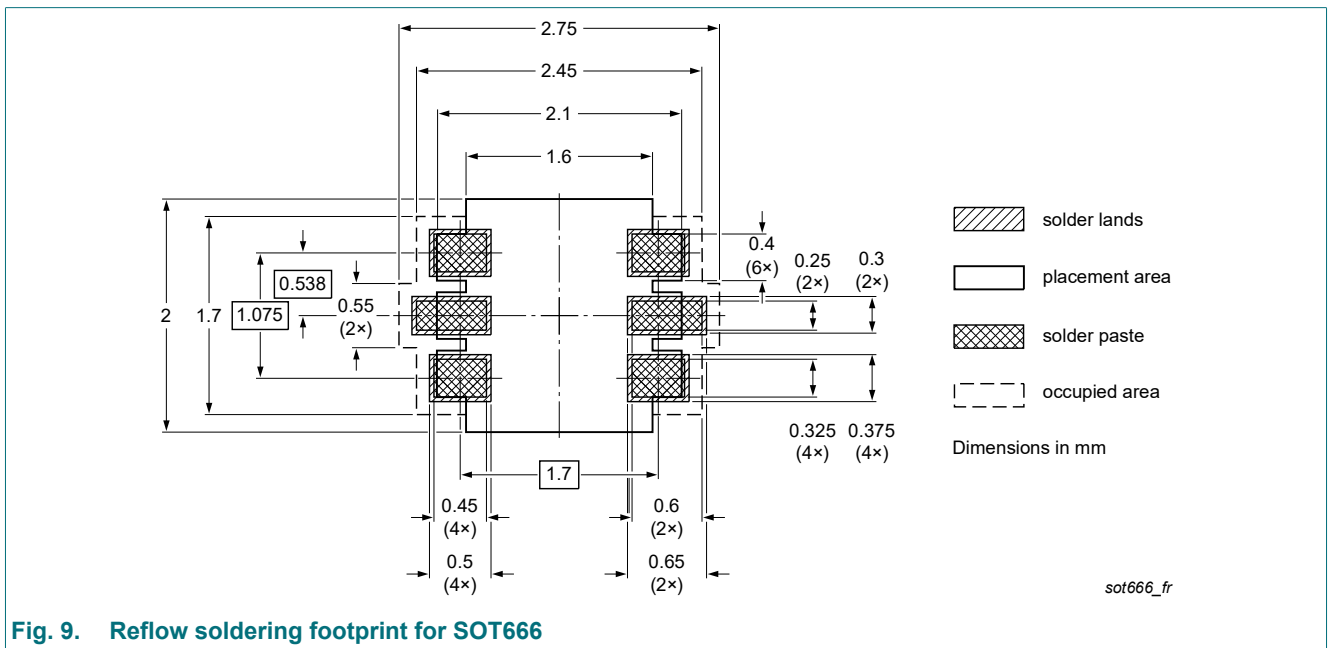


Fig. 9. Reflow soldering footprint for SOT666



## 14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMB24 v.3	20230710	Product data sheet	-	PEMB24_PUMB24_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Family data sheet reduced to single type data sheet.</li> <li>Package information removed.</li> <li>Product(s) changed to non-automotive qualification.</li> </ul>			
PEMB24_PUMB24_2	20090902	Product data sheet	-	PEMB24_PUMB24_1
PEMB24_PUMB24_1	20050218	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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